Furthermore, the device **100** includes first and second metal field plates **160** and **170** for electrical connection and shielding. The field plates **160**, **170** may be electrically isolated from undesired electrical contact with each other and with the rest of the device by one or more insulating layers, e.g., oxide layers, as is commonly done.

FIG. **1**C and FIG. **1**D illustrate an example in which a Zener diode **110** is integrated onto the same substrate as a JFET **180**. In example shown in FIG. **1**D, the JFET **180** is an N-channel JFET. However, aspects of the present disclosure are not limited to such implementations. The Zener diode **110** in FIG. **1**D has the same structure as the Zener diode **110** of FIG. **1**B. The JFET **180** includes a bottom gate **181**, a source **182**, a floating top gate **183**, and a high voltage N-well (HVNW) that acts as an extended drain **184**. The bottom gate **181** includes a P+ region inside a P-well at an outer edge of the device. The bottom gate **181** is electrically connected to ground potential, as shown in FIG. **1**C. The source **182** is formed in the epitaxial layer **104** from an N+ region inside an N-well between the bottom gate **181** and the top gate **183**. The source **182** is electrically connected to a portion of the upper metal layer **170** that acts as a source electrode and field plate. The top gate **183** includes a P+ region inside a less heavily doped P-well formed in the HVNW **184** under a portion of the metal layer **160** that acts as a top gate electrode. A gate voltage may be applied to the top gate **183** through an electrical connection (not shown). An N-channel **185** is formed in the HVNW **184** under the top gate **183** when the gate voltage is applied to the top gate. The JFET **180** is isolated from the Zener diode by a structure similar to that shown in FIG. **1**B.

A similar N-well **108** and an (optional) NBL **187** may be formed under a doped region **186** that acts as the drain contact for the JFET **180**. The NBL **187** may be omitted, if the electric field at the edge of the transistor **180** does not have to be relaxed. The drain contact **186** may be connected to the anode **124** of the Zener diode **110** through a portion of the lower metal layer **160**.

As discussed above, FIG. **2**B illustrates portions of a device integrating two Zener diodes **110**, **110**A with a transistor according to one embodiment of the present disclosure.

Similar to FIG. **1**B. Elements common to FIG. **1**B and FIG. **2**B are indicated by the same or similar reference numerals. In addition to a Zener diode **110** the device depicted in FIG. **2**B includes a second diode **110**A along with the depletion-mode transistor **130**. As with the device of FIG. **1**B, the Zener diodes **110**, **110**A and transistor **130** are formed in a P-type epitaxial layer **104** over a P-type substrate **102**. Zener diode **110** may be configured as discussed above with respect to FIG. **1**A. Likewise the second Zener diode **110**A may include an N-type well **112**A and a P-type well **122**A formed in the P-type epitaxial layer **104**. An N^+ region **114**A that serves as the cathode of the diode **110**A and a P^+ region **124**A that serves as the anode of the diode **110**A are encompassed in a P-type well region **126**A in the P-type well **122**A. These regions may be formed by ion implantation process known in the art to dopant concentrations within the ranges described above with respect to corresponding regions in FIG. **1**A. The anode **124** of the Zener diode **110** may be connected to the cathode **114**A of the second Zener diode **110**, e.g., by a metal structure **161**, which can be part of the same metal layer as the field plate **160**. The diodes **110**, **110**A may be isolated by an isolation structure having an N-type buried layer (NBL) **106** underneath both diodes and individual isolation structures including N-type wells **108**, **108**A on top of the NBL **106**, and HVNW **109**,**109**A over the N-type wells. As with the device of FIG. **1**B, the NBL **106** is formed between the P-type substrate **102** and the P-type epitaxial layer **104**. One N-type well **108**A and HVNW **109**A are formed between the two diodes **110**, **110**A and another N-type well **108** and HVNW **109** are formed between the second diode **110**A and the transistor **130**.

It is noted that the device of FIG. **1**D may be similarly modified to incorporate two Zener diodes in the manner shown in FIG. **2**B.

FIG. **3**A-**3**C are top views of a device of FIG. **1**B according to an aspect of the present disclosure. FIG. **3**A is a top view of a device of FIG. **1**B showing the structure in the P-type epitaxial layer **104** and the gate **134**. FIG. **3**B is a top view of a device of FIG. **1**B showing the metal field plates **160** and **170**. FIG. **3**C is a top view of a device of FIG. **1**B showing NBL **106** and P-Epi **104**. As can be seen from these drawings, the device in FIG. **1**B is circularly symmetric about the cathode **114** of the Zener diode **110**, which is connected to drain potential. The other regions of the device are formed in concentric rings with the cathode **114** at the center. The devices shown in FIG. **1**C and FIG. **2**B may be similarly circularly symmetric. Although circularly symmetric devices are described herein, those skilled in the art will appreciate that other types of symmetry may be used.

Devices of the type described herein may be fabricated by forming depletion device or junction field effect transistor (JFET) having a drain connected in series with the one or more Zener diodes by forming a plurality of doped regions of the type described herein in the same P-type semiconductor substrate and separated by a punch through stop region. The key step is forming a first N-type region **106** in the substrate under the one or more Zener diodes and (optionally) a second N-type region **137** in the substrate under the depletion device or JFET **130** with the first and second N-type regions are separated by the punch through stop **152**. The various doped regions may be formed in any suitable order depending on the doping techniques used. For example, a high energy implant may be used to form the buried N-type regions **106**, **137** under the one or more Zener diodes **110**, **110**A. Alternatively, N-type regions **106**, **137** may be formed before forming the doped regions located above them. In such a case, the buried N-type regions may be formed directly into the P-type substrate **102** and the epitaxial layer **104** may be omitted.

In such implementations, doped regions that are described as being formed in the epitaxial layer **104** may be formed directly into the substrate **102**. Alternatively, the N-type regions may be formed by more conventional implant into the substrate **102** before forming the epitaxial layer **104**. This may be followed by a heating step to diffuse the dopants vertically into the epitaxial layer.

Although the above examples are described for a device formed on a P-type substrate, aspects of the present disclosure include implementations in which P-type and N-type are switched.

While the above is a complete description of the preferred embodiments of the present invention, it is possible to use various alternatives, modifications, and equivalents.

Therefore, the scope of the present invention should be determined not with reference to the above description but should, instead, be determined with reference to the appended claims, along with their full scope of equivalents. Any feature, whether preferred or not, may be combined with any other feature, whether preferred or not. In the claims that follow, the indefinite article "A" or "An" refers to a quantity of one or more of the item following the article,